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New Orleans, Louisiana, United States  
Pages: 794 - 797  
Year of Publication: 1999  
ISBN:1-58133-109-7

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**Sponsors** EDAC : Electronic Design Automation Consortium  
IEEE-CAS : Circuits & Systems  
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**Publisher** ACM Press New York, NY, USA

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1 [P. Bellows , B. Hutchings, JHDL - An HDL for Reconfigurable Systems, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, p.175, April 15-17, 1998](#)

2 [Peter Clarke: Tricore to get flash FPGA integration. In EE Times, No. 1000; CMP Media, 1998.](#)

3 [Josef Fleischmann , Klaus Buchenrieder , Rainer Kress, A hardware/software prototyping environment for dynamically reconfigurable embedded systems, Proceedings of the 6th international workshop on Hardware/software codesign, p.105-109, March 15-18, 1998, Seattle, Washington, United States](#)

4 [Rachid Helaihel , Kunle Olukotun, Java as a specification language for hardware-software systems, Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design, p.690-697, November 09-13, 1997, San Jose, California, United States](#)

5 [JavaBeans API specification, Sun Microsystems, http://java, sun.com/beans, 1998.](#)

- 6 Asawaree Kalavade , Pratyush Moghé, A tool for performance estimation of networked embedded end-systems, Proceedings of the 35th annual conference on Design automation, p.257-262, June 15-19, 1998, San Francisco, California, United States
- 7 T. Kuhn, W. Rosenstiel: Java Based Modeling and Simulation of Digital Systems on Register Transfer Level. In Workshop on System Design Automation, 1998.
- 8 Eric Lechner , Steven A. Guccione, The Java environment for reconfigurable computing, Proceedings of the 7th International Workshop on Field-Programmable Logic and Applications, p.284-293, September 01-03, 1997
- 9 National Semiconductor: Napal000 Adaptive Processor, <http://www.national.com/appinfo/milaero/napal000>, 1998.
- 10 Stuart Nisbet , Steve Guccione, The XC6200DS development system, Proceedings of the 7th International Workshop on Field-Programmable Logic and Applications, p.61-68, September 01-03, 1997
- 11 R. Passerone, et al.: Modeling Reactive Systems in Java. In Int. High Level Design Validation and Test Workshop, Nov. 1997.
- 12 M. Vasilko: Dynamically Reconfigurable Hardware WWW Library, Bournemouth University, <http://dec.bournemouth.ac.uk/drhwl-lib/>
- 13 James Shin Young , Josh MacDonald , Michael Shilman , Abdallah Tabbara , Paul Hilfinger , A. Richard Newton, Design and specification of embedded systems in Java using successive, formal refinement, Proceedings of the 35th annual conference on Design automation conference, p.70-75, June 15-19, 1998, San Francisco, California, United States

## ↑ CITINGS

Roman Lysecky , Frank Vahid, Prefetching for improved bus wrapper performance in cores, ACM Transactions on Design Automation of Electronic Systems (TODAES), v.7 n.1, p.58-90, January 2002

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↳ D.4.7 Organization and Design

↳ **Subjects:** Real-time systems and embedded systems

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**2 A bitstream reconfigurable FPGA implementation of the WSAT algorithm**

*Leong, P.H.W.; Sham, C.W.; Wong, W.C.; Wong, H.Y.; Yuen, W.S.; Leong, M.P.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume:

9 , Issue: 1 , Feb. 2001

Pages:197 - 201